Scheduling Problems in Semiconductor Wafer Fabrication Facilities: Part 1

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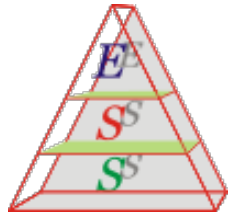


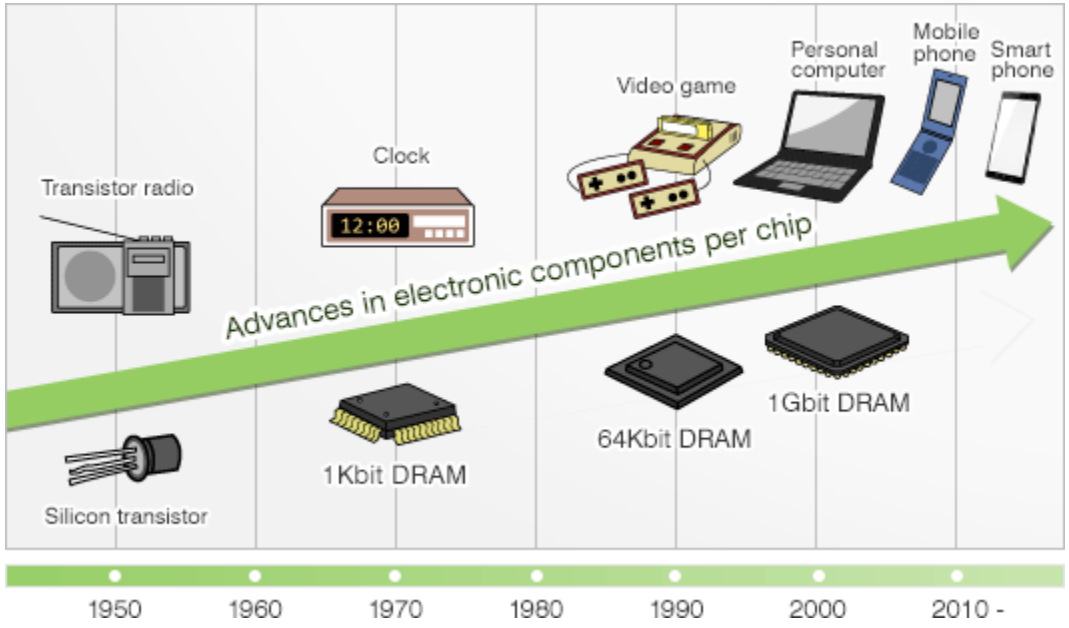
Agenda

- Motivation
- Process Description
- Scheduling Problems
- Factory Scheduling — **Part 1**

- Batch Scheduling Problems — **Part 2**
- Multiple Orders per Job Scheduling Problems — **March 16**
- Scheduling Jobs with Time Constraints
- Conclusions and Future Challenges

Motivation

- Semiconductors are ubiquitous

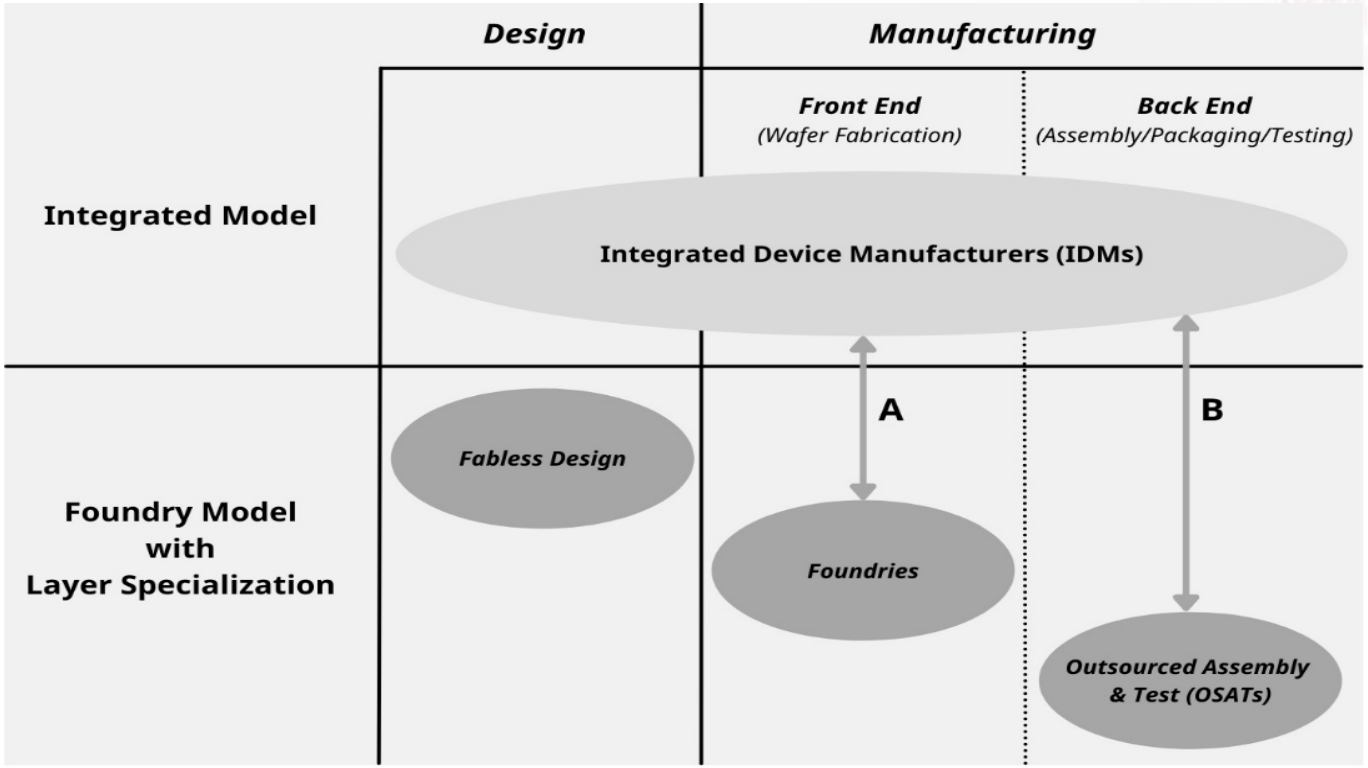


- 2021 Global semiconductor industry sales were US$555.9 billion[1]

[1]Semiconductor Industry Association (SIA)

Motivation

- Semiconductor Industry Business Models



A: IDMs utilize foundries for some manufacturing
B: IDMs utilize OSATs for some assembly/packaging/testing

Motivation

- Manufacturing integrated circuits is complex and costly
  - TSMC's new fab will cost US$12B and take over 2 years to bring online
- Scheduling problems attracted researchers and practitioners for the last three decades
- Causes: high degree of automation even 30 years ago
  - automated real-time data collection
  - manual production control leads often to unexpected behavior of the system
- Increasing automation pressure by automated material handling systems (AMHS) and new requirements on production control

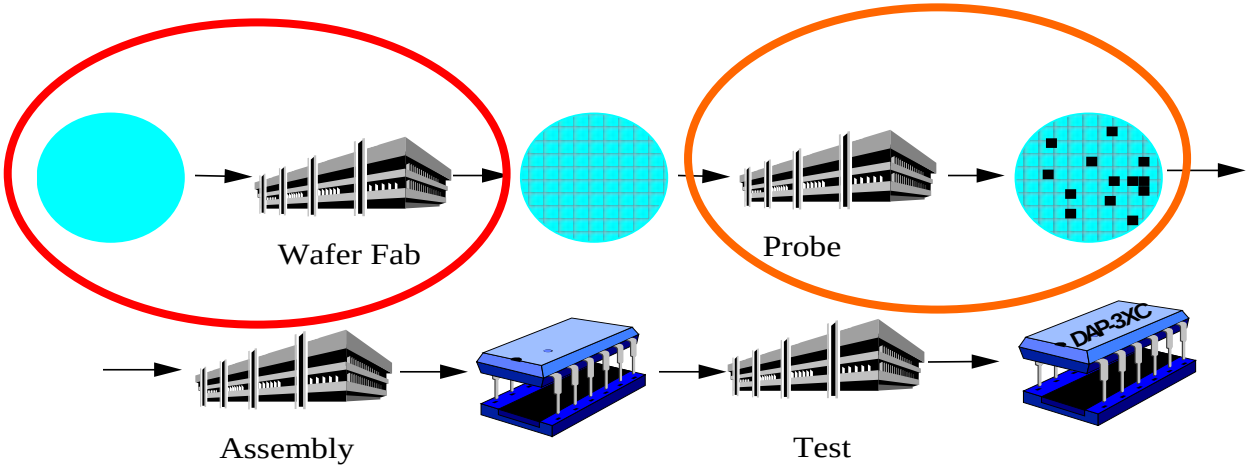
=> Scheduling approaches are both promising and necessary in the semiconductor domain

- Current state of the art in this industry:
  - **Sophisticated dispatching rule-based systems**
  - **Optimization approaches for individual workcenters**

Process Description

- Semiconductor chip = highly miniaturized, integrated electronic circuit consisting of thousands of components
- Raw wafers = thin discs made of silicon or gallium arsenide
- Up to thousand identical chips can be made on each wafer.
  1. The electronic circuits are build up layer by layer in a **Wafer fab**.
  2. Then the wafers are sent to **Probe**, where electrical tests identify any die that is not good when packaged.

Front-end = Wafer fab + Probe

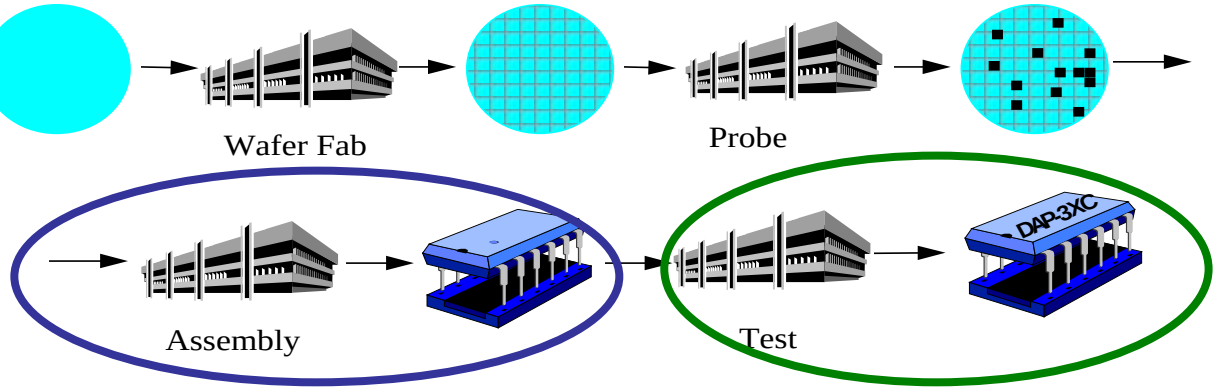


Process Description

3. Probed wafers are sent to **Assembly** where good dies are put into a package.
4. Packaged dies are sent to **Test** where they are tested before they are going to customers.

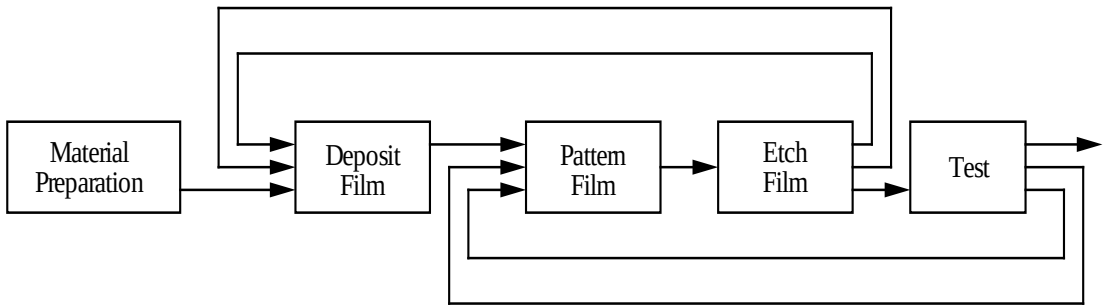
Back-end = Assembly + Test

- In this talk => We consider mainly the wafer fab part of the manufacturing process.



Process Description

- Many process flows
- Each process flow contains up to 1200 steps
- Several hundred (often very expensive) machines
  - A state-of-the-art lithography machine costs ~US$150M
- Unrelated parallel machines
- Re-entrant flows
- Different processing times



Process Description

- Wafer Processing times can be wafer-, lot-, or batch-based
- Long operations often involve batch processes (one third of all operations might be batch operations)
- Non-linear flow because of mixture of batching and non-batching machines => long queues in front of the machines
- Nested time constraints for the processing of jobs to prevent native oxidation and contamination effects on the wafer surface
- Probabilistic occurrence of long machine failures leads to large variability

Process Description

- Some machines like implanters require significant sequence-dependent setup times
- Dynamic bottlenecks depending on the product mix
- Some processing steps require auxiliary resources such as reticles in photolithography
- Wafers are transported in Front Opening Unified Pods (FOUP) using an AMHS => manual handling of the wafers is not desirable

⇒ **Manufacturing environment that is different in several ways from traditional flow and job shops**

Scheduling Problems

- Batch = group of jobs that have to be processed together
- Completion time of a batch = completion time of the last job of the batch

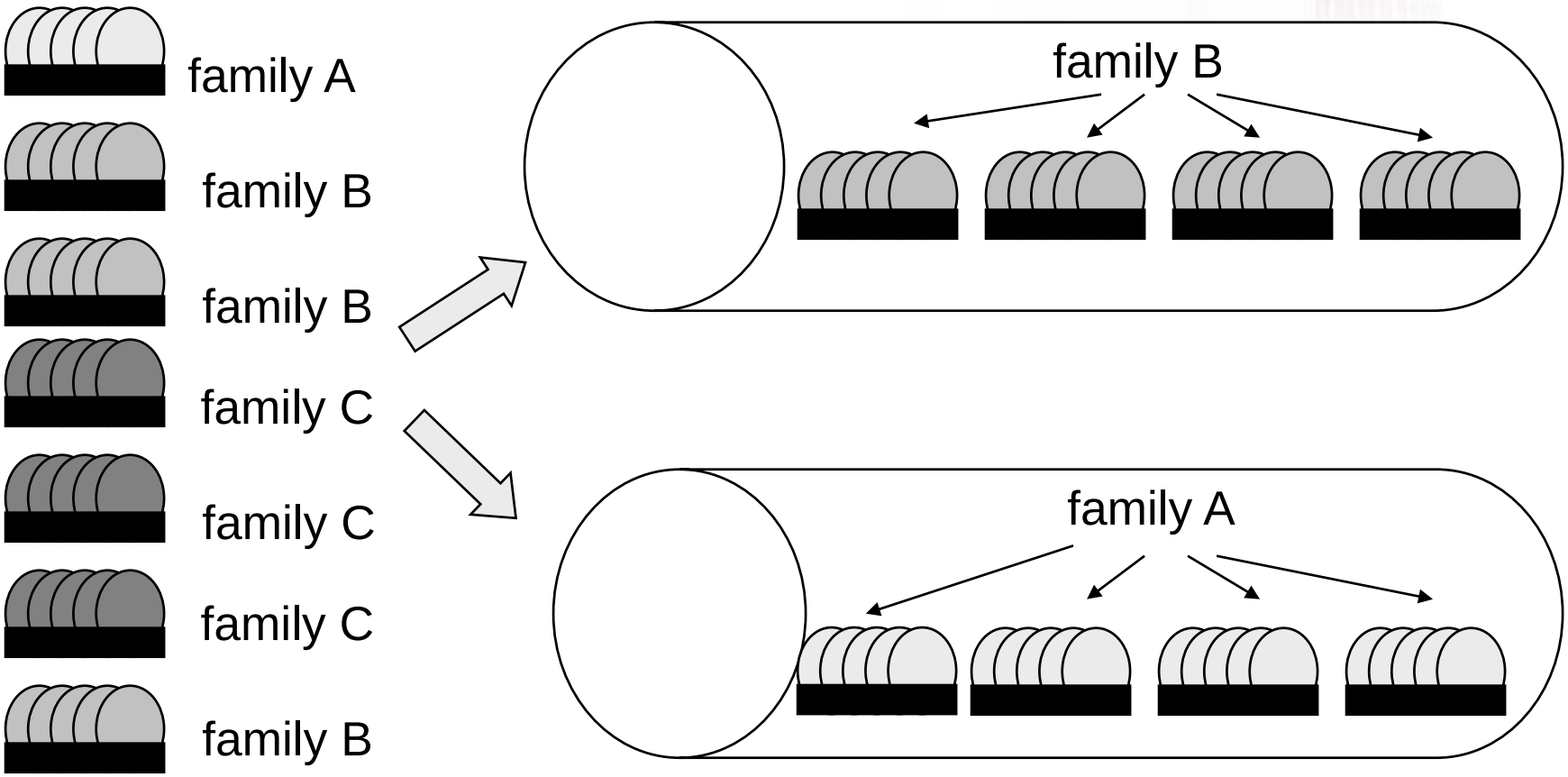
- Two types of batching problems:
  - s-batching: processing time of the batch is the **sum** of the processing time of the jobs
  - p-batching: processing time of the batch is the maximum processing time of the jobs that form the batch
- p-batching is very important in semiconductor manufacturing.

- Assumption of a fixed batch size B
  - burn-in ovens are used to heat-stress test chips
  - diffusion furnaces => incompatible job families, only jobs of one job family can be batched together due to the chemical nature of the process

- In some cases secondary resources are required for batching machines (load boards, reticles)

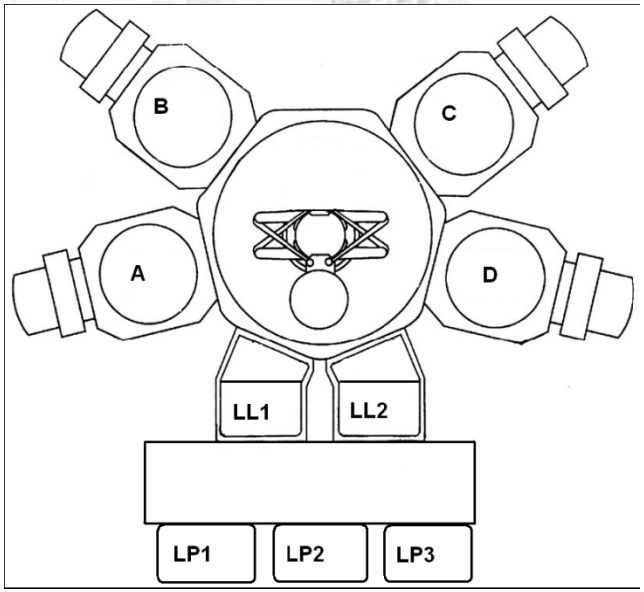
Scheduling Problems

Example: three incompatible families, B=4



Scheduling Problems

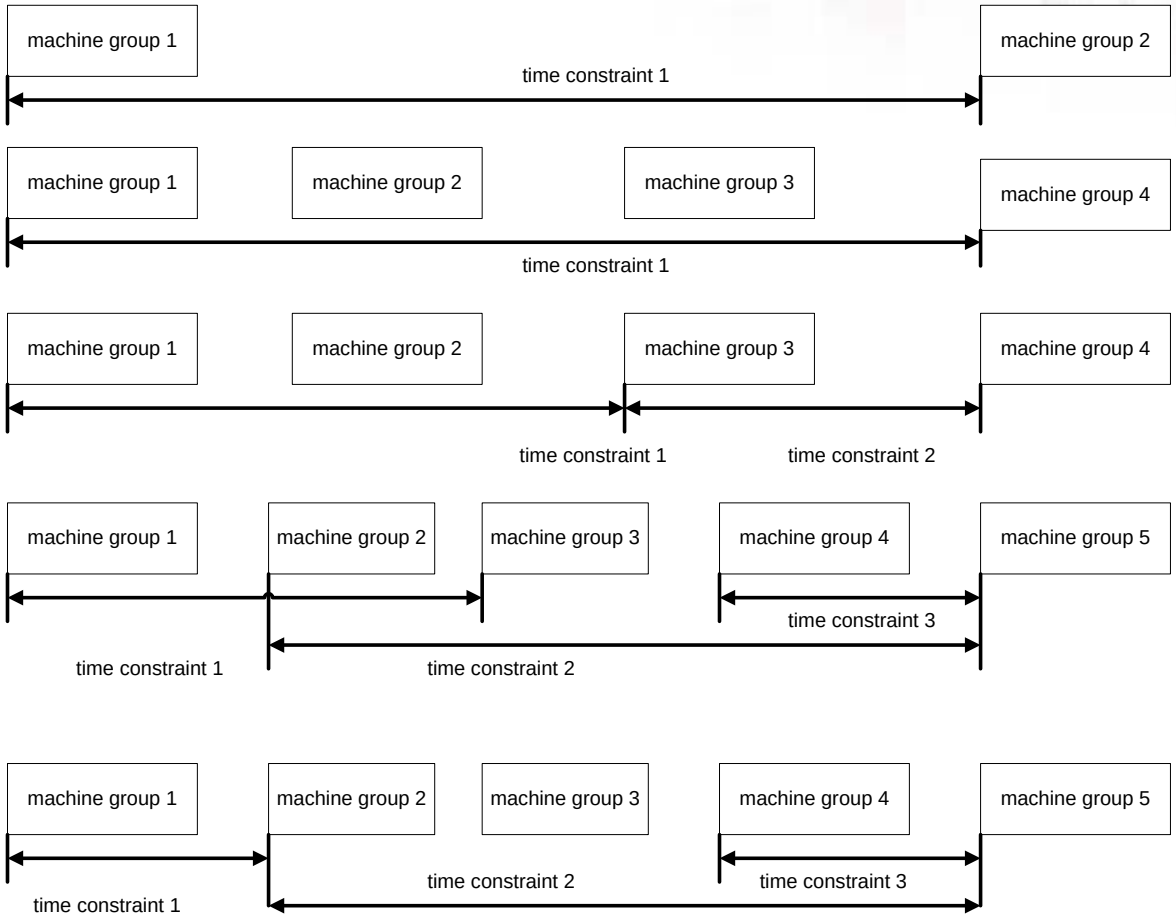
- **Cluster tools** combine single wafer processing with wafer handling robots in one closed environment.
- **Example**
  - three load ports LP1,LP2,LP3 where lots are deposed (three lots)
  - wafers are transported to the two load locks LL1, LL2 (two wafers)
  - wafers are transferred to one of the four processing chambers A,B,C,D by a two-armed robot



- **Scheduling of cluster tools** is challenging because of the cycle time of wafers in a cluster tool depends on the used wafer recipes, cluster tool control and architecture, wafer waiting times, and sequencing

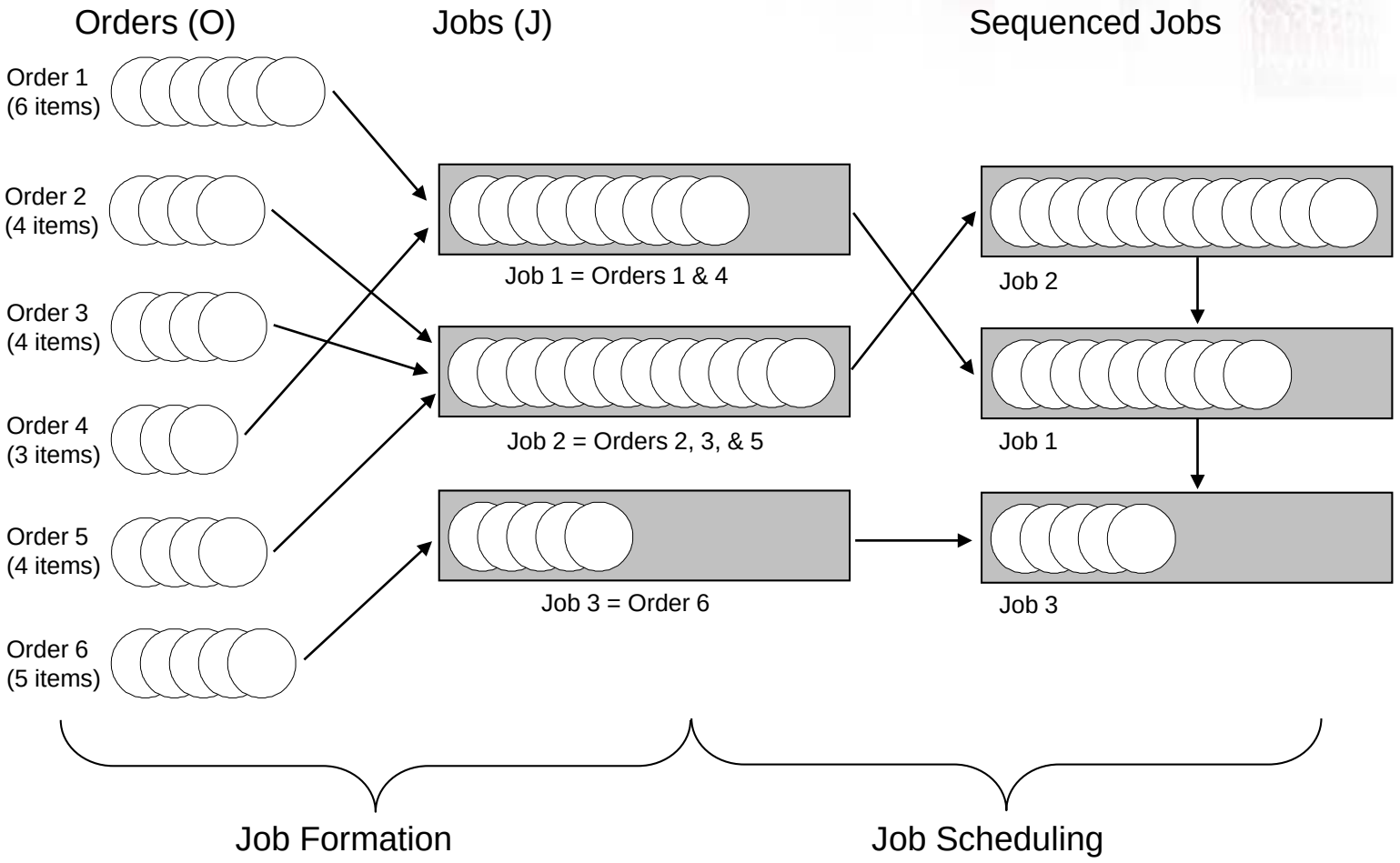
Scheduling Problems

- Time constraints take on many forms



Scheduling Problems

▷Multiple orders per job problems



Scheduling Problems

- Wafer fabs can be modeled as complex job shops (Ovacik & Uzsoy, 1997):
  - unrelated parallel machines with sequence-dependent setup times
  - parallel batch machines, re-entrant flows
  - ready times of the jobs
- $FJm \mid r_j, \text{p} - \text{batch}, \text{incompatible}, s_j, recrc \mid \sum w_j T_j$ (1)
- $FJm \mid r_j, \text{p} - \text{batch}, \text{incompatible}, s_j, recrc \mid L_{\max}$ (2)
- **Disjunctive graph formulations** to solve (1) and (2) => shifting bottleneck heuristic
- Large-scale job shops: several hundred machines, several hundred jobs, diverse production mix

ASU Arizona State University

A Deterministic Scheduling Approach for Wafer Fabrication Facilities

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Mason, S.J., Fowler, J.W. and Matthew Carlyle, W., 2002. A modified shifting bottleneck heuristic for minimizing total weighted tardiness in complex job shops. *Journal of Scheduling*, 5(3), pp.247-262.

FORCe Scheduling

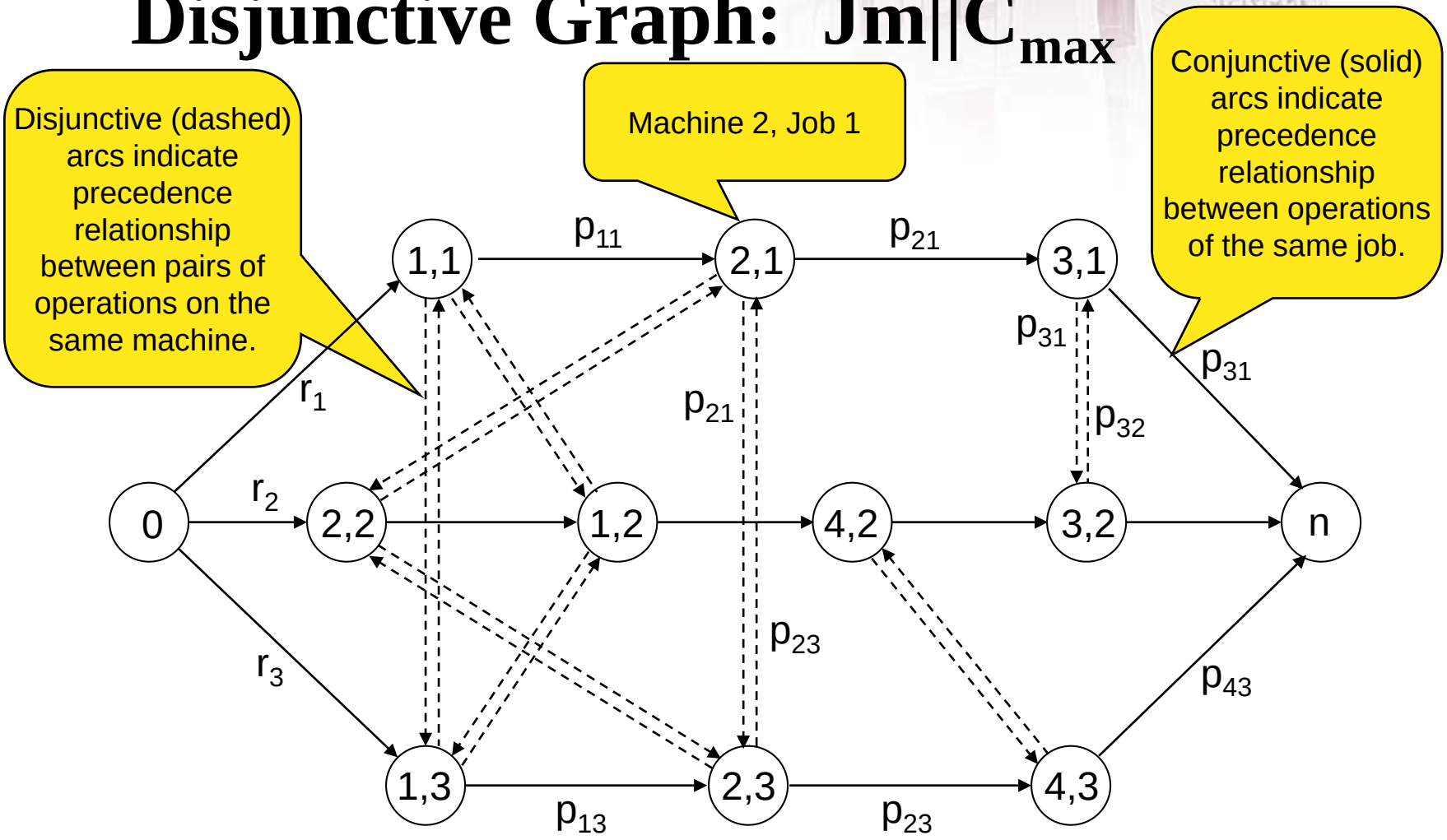
- Project Goal:
  - To develop a deterministic scheduling approach that is capable of handling global scheduling decisions in a fab and performs well under uncertainty.

- Project funded by:
  - Factory Operations Research Center (FORCe)
  - International Sematech
  - Semiconductor Research Corporation

The Classical Job Shop: $Jm||C_{max}$

- Characterized by sequencing n jobs on m machines in order to minimize the total time required to process all jobs (makespan or $C_{\max}$)
- Large computational effort associated with obtaining exact solutions to real-world problems
  - Potential for $(n!)^m$ different schedules to be evaluated
  - $Jm \,||\, C_{\max}$ is **NP**-hard (Garey, Johnson, and Sethi, 1976)
  - For 6 jobs and 5 machines, over 193 trillion schedules exist
- Many of the heuristics successfully applied to the $Jm \,||\, C_{\max}$ problem are based on a disjunctive graph approach.

Disjunctive Graph: $Jm||C_{max}$



The Shifting Bottleneck Procedure

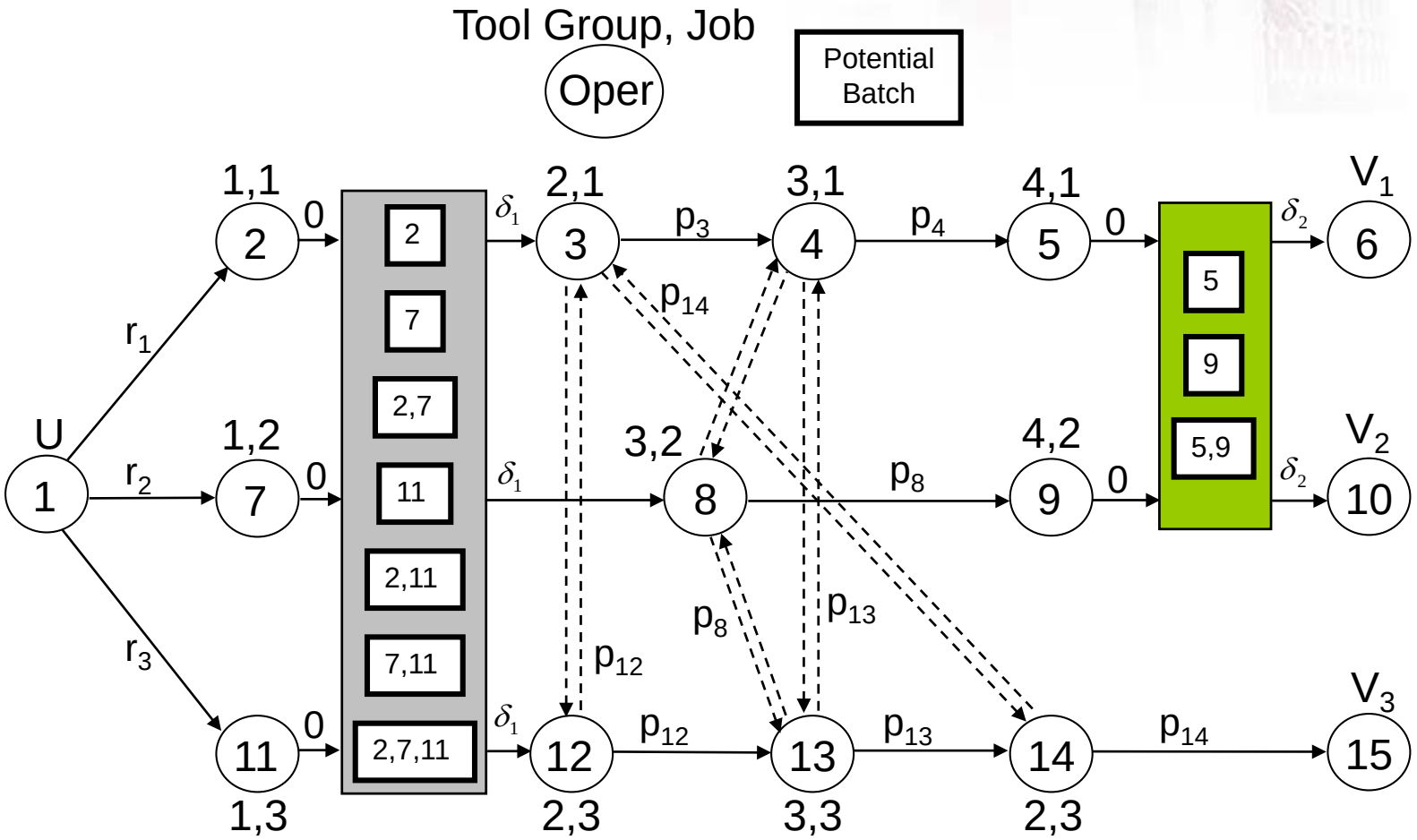
- $Jm \,||\, C_{\max}$ problems are frequently analyzed using the Shifting Bottleneck (SB) procedure (Adams, Balas, Zawack, 1988).

- SB decomposes $Jm \,||\, C_{\max}$ into multiple instances of the $1 \,|\, r_j \,|\, L_{\max}$ problem ("subproblems")
  - Subproblems solved according to some specified "subproblem solution procedure" (SSP), then evaluated in terms of a specified performance or "machine criticality" measure (MCM).
  - The "most critical" or bottleneck machine is scheduled at each iteration of SB.
  - Using this decomposition technique, key sections (tools) of problem (factory) can be considered in order of importance.

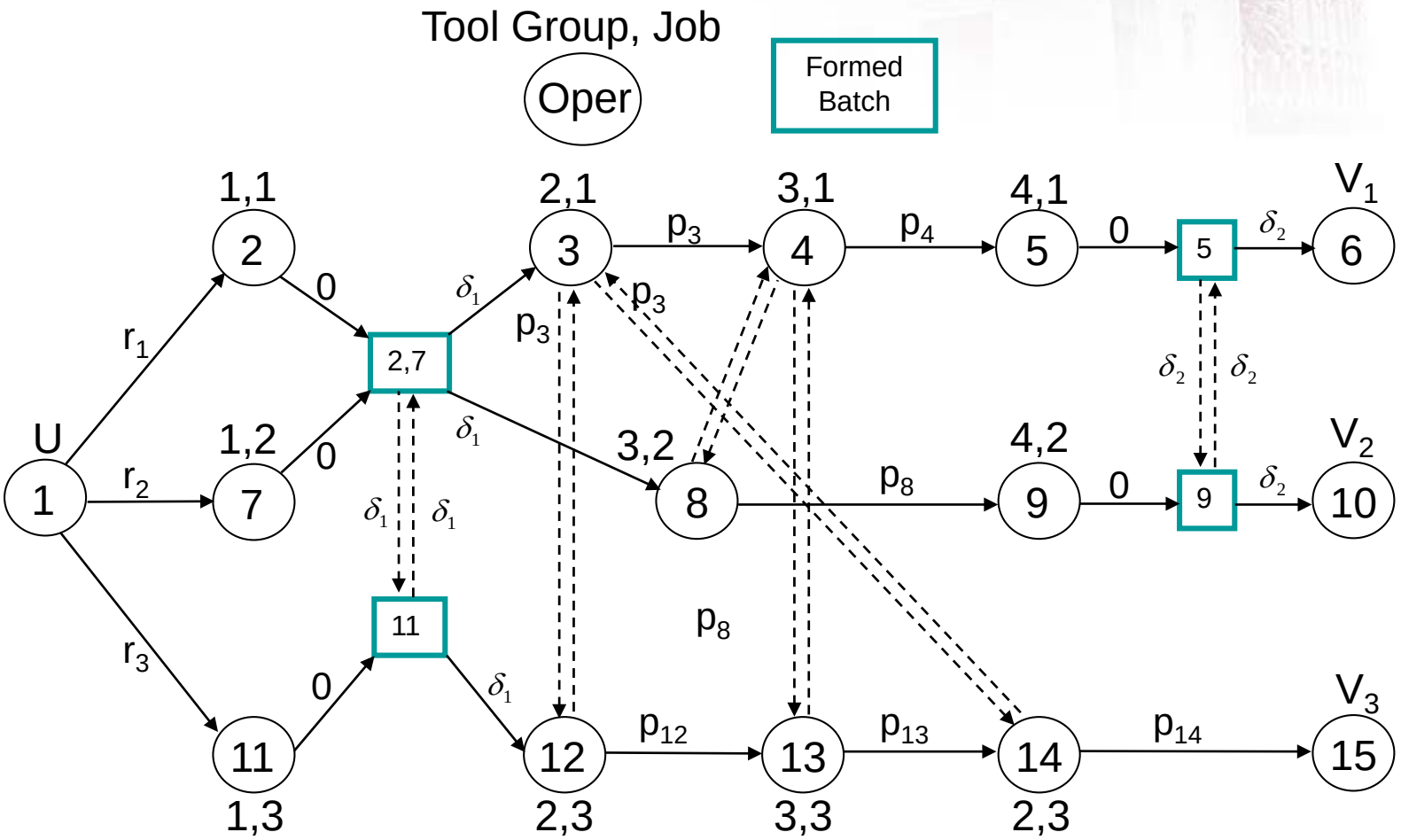
Minimizing Total Weighted Tardiness in Complex Job Shops

- Job j 's lateness $L_j = C_j - d_j$
- Job j 's tardiness $T_j = \max(C_j - d_j, 0)$
- Can scale each job's tardiness by it's priority or weight w_j, then sum to compute total weighted tardiness ($\sum w_j T_j$)
- Pinedo and Singer (1999) investigated $Jm \mid r_j \mid \sum w_j T_j$
- Existence of ready times, recirculating flow, batching tool groups, and sequence-dependent setups results in $FJc \mid r_j, s_{jk}, B, recrc \mid \sum w_j T_j$

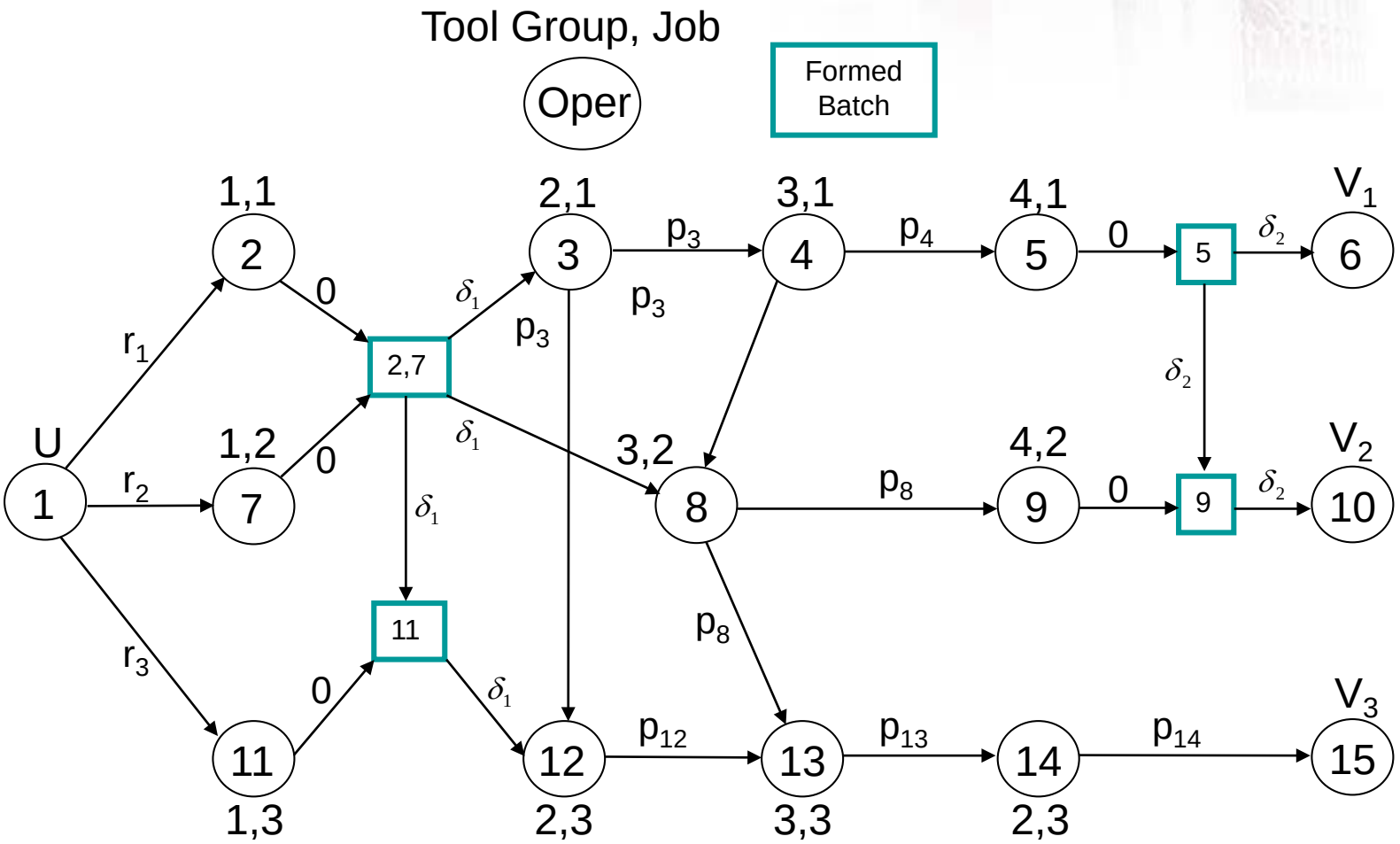
Disjunctive Graph: $FJc|r_j,s_{jk},B,recrc|\Sigma w_j T_j$



Disjunctive Graph: Batch Formation



Feasible Schedule for $FJc|r_j,s_{jk},B,recrc|\Sigma w_j T_j$



Heuristic for Minimizing TWT in Complex Job Shops

1. Let M = the set of all m tool groups and M_o = the set of tool groups that have been sequenced or scheduled. Set $M_o = \emptyset$.

2. Identify and solve the subproblems for each tool group $i \in M \setminus M_o$ using a **SSP**.

3. Identify a critical or bottleneck tool group $k \in M \setminus M_o$ using a **MCM**.

4. Sequence tool group k using the solution from the SSP in Step 2. Set $M_o = M_o \cup \{k\}$.

5. Optional: Reoptimize the schedule for each tool group $i \in M_o \setminus \{k\}$, considering the newly added conjunctive arcs for tool group k.

6. If $M = M_o$, stop. Otherwise, go to Step 2.

Case Study: A Wafer Fab Model Static Instances

- Testbed Dataset 1 (https://p2schedgen.fernuni-hagen.de/index.php?id=simulation&L=1) was used to evaluate TWT of schedules produced by five dispatching rules and the modified SB heuristic (SBH)

- Dispatching rules investigated were
  - Priority-based First-In/First-Out (PRFIFO)
  - Least Slack (LSLACK)
  - Priority-based Critical Ratio (PCR)
  - Priority-based Earliest Due Date (PREDD)
  - Shortest Processing Time (SPT)

Case Study: A Wafer Fab Model

- Using Dataset 1, the top 10 bottleneck tools that cost over $100,000 identified using Factory Explorer
  - Created modified version of dataset containing top 10 bottleneck tools and simulated process delay steps for all other tools' assigned steps

- As only a percentage of Dataset 1's production volume will be used in the comparative analysis, the tool set quantities need to be reduced such that critical or bottleneck tools still existed in our experimental test cases.
  - The revised quantity of tools in each tool group was determined using the daily going rate (DGR) as calculated by Factory Explorer.
    - A tool's DGR is defined as the sum of product throughput rates divided by the tool's capacity loading (Wright Williams & Kelly 2000).

Case Study: A Wafer Fab Model

- A sequence-dependent setup matrix was established for the dataset's ion implantation tools (medium- and high-current)

Current Species	Proposed Species P	As	BF_2	B
P	-	45	75	60
As	45	-	60	75
BF_2	45	30	-	45
B	30	45	45	-

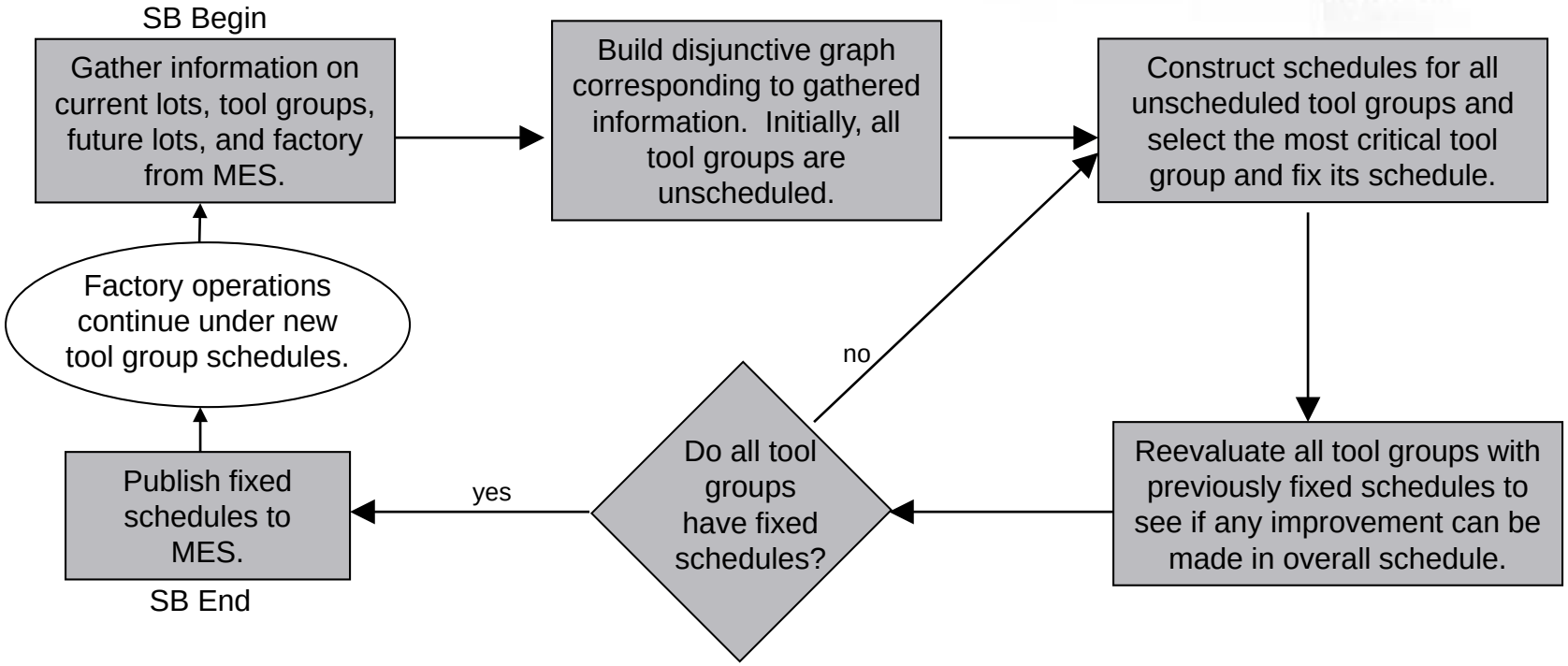
- Investigated ten different 20-job instances of modified Dataset 1 model with random ready times, weights, and due dates

Case Study Results

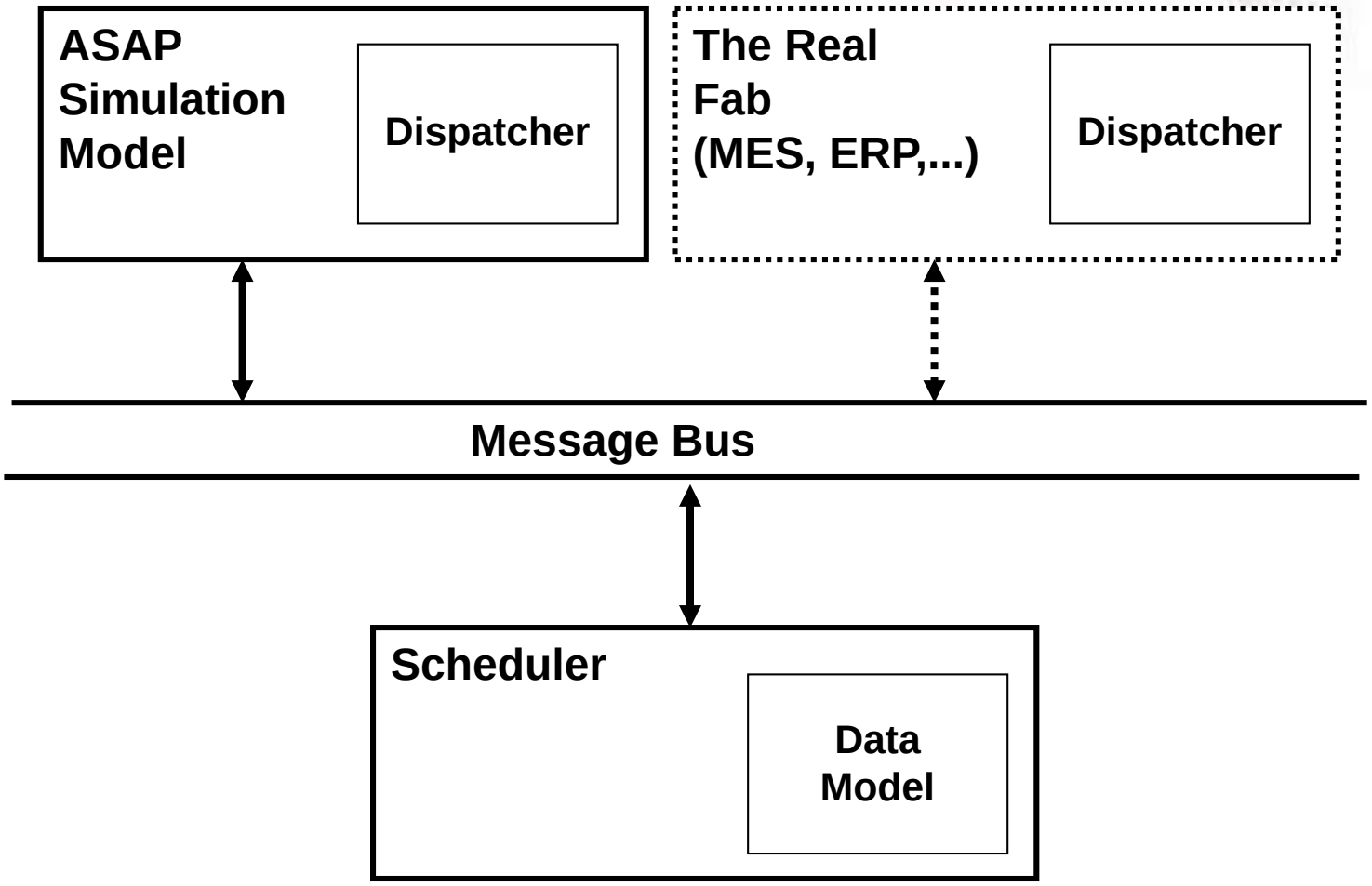
- For each case, the values below represent the ratio of the TWT solution obtained by the current method to the lowest overall TWT solution (that is, 1.00 is the best solution).

Case	PRFIFO	LSLACK	PCR	PREDD	SPT	SBH
1	1.94	2.61	1.92	1.94	2.50	**1.00**
2	2.29	2.62	2.25	2.27	3.40	**1.00**
3	**1.00**	1.16	**1.00**	**1.00**	1.16	2.68
4	1.52	1.97	1.24	1.37	2.54	**1.00**
5	1.37	1.88	1.37	1.37	1.79	**1.00**
6	2.57	3.25	2.59	2.63	2.87	**1.00**
7	1.60	1.95	1.59	1.60	1.77	**1.00**
8	1.67	1.92	1.67	1.67	1.85	**1.00**
9	2.44	3.01	2.44	2.43	2.64	**1.00**
10	2.10	2.39	2.09	2.10	2.37	**1.00**
Avg	1.75	2.21	1.71	1.74	2.29	1.24
Var	0.30	0.46	0.33	0.33	0.58	0.40

Our Shifting Bottleneck Heuristic



Framework Architecture



Case Study: A Wafer Fab Model Dynamic Instances

- Comparison of Shifting Bottleneck Heuristic (SBH) and dispatching rules
- Dispatch rules: FIFO, EDD, CR, ODD, ATCS
- Fabs:
  - Fab A = MiniFab (5 tools),
  - Fab B = top 11 bottleneck work centers of Fab C (45 tools)
  - Fab C = MIMAC test bed data set 1 (268 tools, no operators, no reticles)
- Simulated interval: 40 (Fab C) to 500 (Fab A & B) days (without warm-up)
- Bottleneck load: approx. 95%
- Due-date setting: tight (close to FIFO dispatch cycle time averages)
- Performance measure: Total weighted tardiness (TWT)

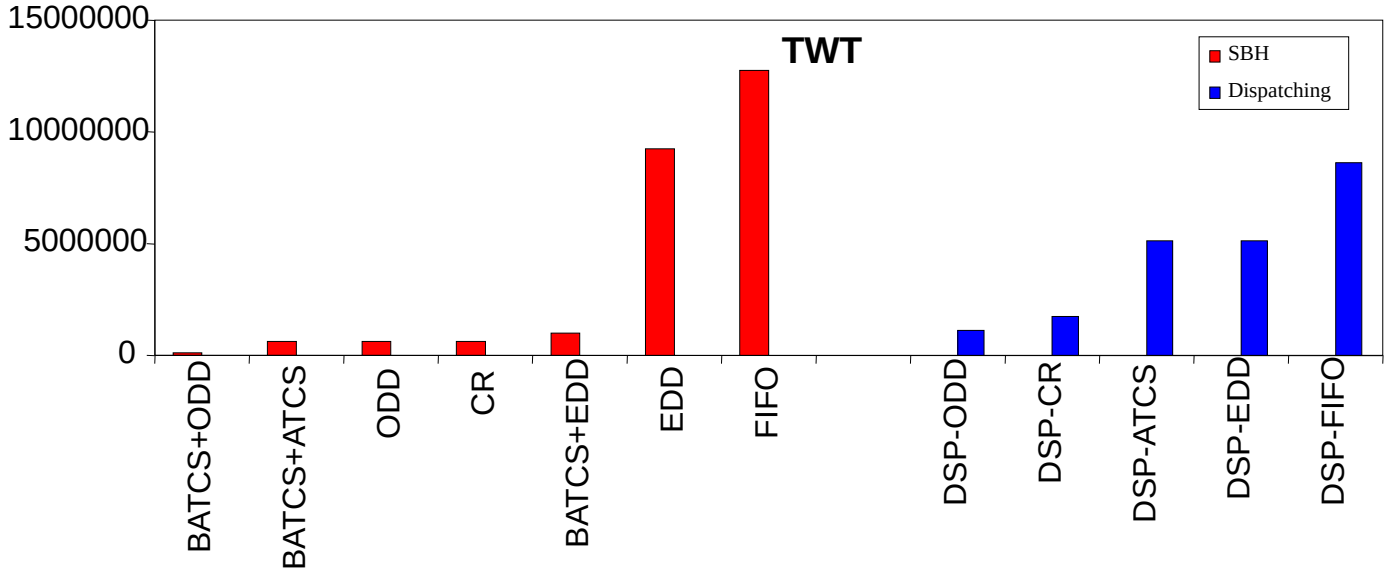
Tested SBH parameters

- Scheduling interval: 2 to 16 hrs
- Additional horizon: 0 to 16 hrs
  - Complete horizon: scheduling interval + additional horizon
- Choice of Subproblem Solution Procedures (SSP): FIFO, EDD, CR, ODD, BATCS (for batch tools) +ATCS (for regular tools), BATCS+CR, BATCS+ODD
- Number of re-optimization steps
- (B)ATCS parameters

Part 1: Fab A & B (small models)

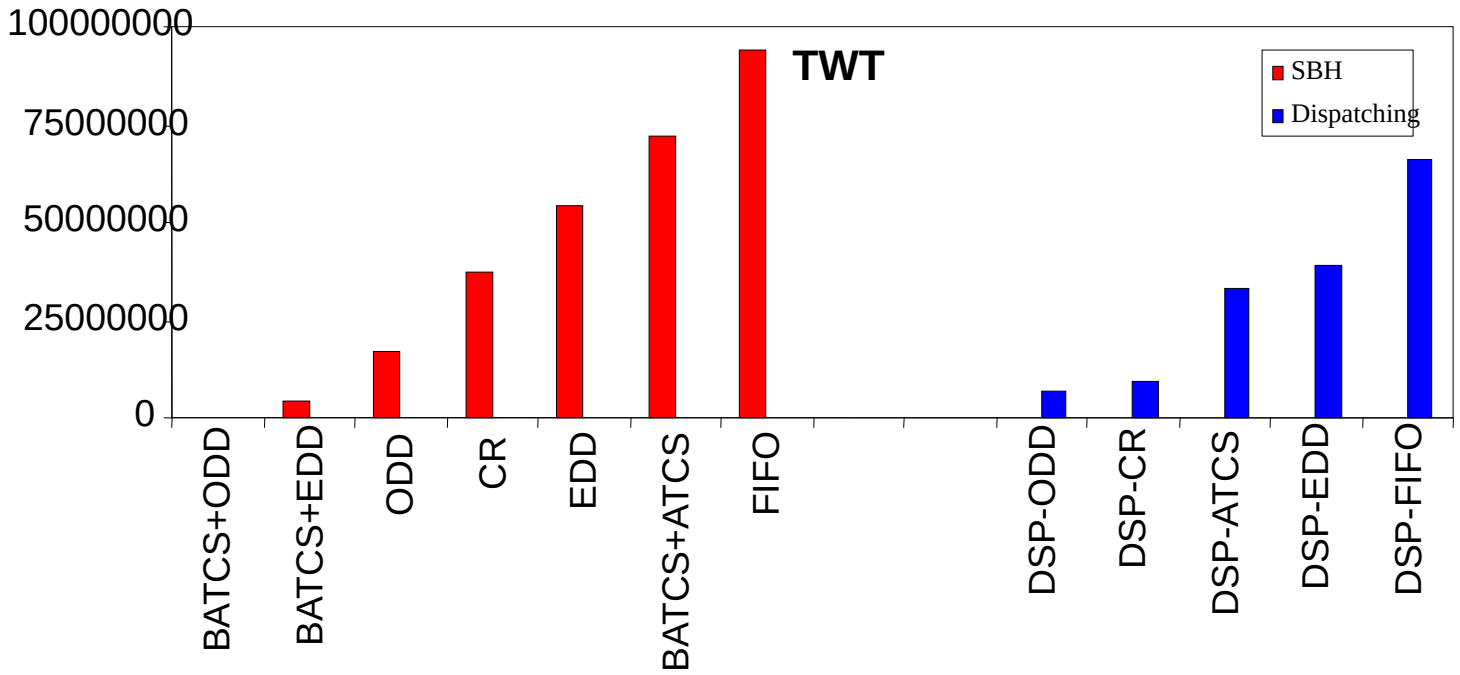
SBH vs Dispatching

- TWT is given in seconds, other parameters set to reasonable/optimal values
- Fab A: best SBH value is 13.4 % of best dispatch value



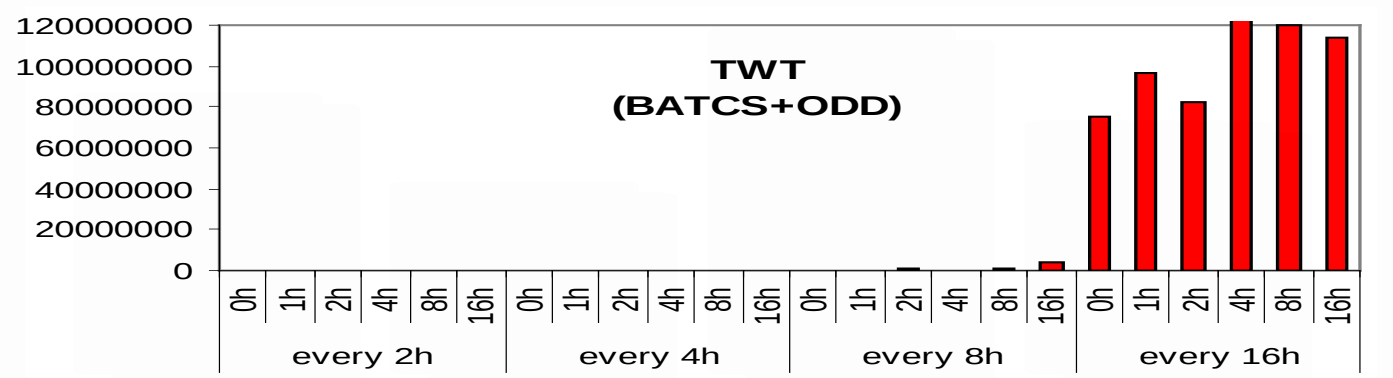
SBH vs Dispatching

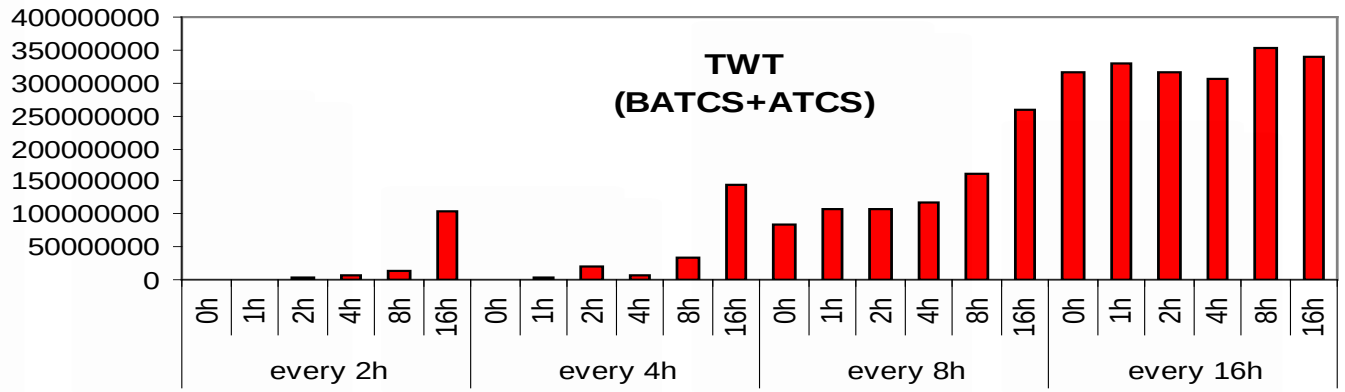
- Fab B: best SBH value .0025 % of best dispatch value



Scheduling interval & additional horizon

- Fab B: Short intervals and short horizons lead to best results





Computation time Fab B

- Fab B: 45 tools in 11 sets, 2 products (56 & 66 steps) @ 95% load
- Automated parameter setting for (B)ATCS
- Standard 2 GHz P4 desktop computer with reasonable amount of memory
- Best TWT case (BATCS+ODD, scheduling interval 2 hrs, no additional horizon): less than .2 seconds per schedule
- Longest computation time found in experiments made (BATCS+ATCS, scheduling interval 2 hrs, 16 hrs additional horizon, leading to bad TWT results): less than 6 minutes per schedule

Part 2: Fab C (large model)

- CR was best dispatch rule for Fab C @ 95% load
- SBH was run with scheduler interval of 2 hrs and no add. horizon

FF	Rule	# lots completed	# late	TWT
1.4 & 1.5	Disp_CR	537	356	8.155.803
	Sched_BATCS/ATCS	561	52	2.844.991
	Sched_BATCS/ODD	567	56	2.854.545
1.47 & 1.66	Disp_CR	536	0	0
	Sched_BATCS/ATCS	561	1	22.100
	Sched_BATCS/ODD	567	2	27.918

Computation time Fab C

- 268 tools in 84 sets, 2 products (210 & 245 steps) @ 95% load

- Best TWT case (BATCS+ATCS, scheduling interval 2 hrs, no additional horizon): less than 50 seconds with automated parameter setting, less than 13 seconds with given (B)ATCS parameters

Conclusions

- With reasonable parameters the Shifting Bottleneck Heuristic clearly outperforms classical dispatching approaches like Critical Ratio with respect to on-time delivery performance
- To generate good schedules the SBH horizon should be kept small (2 hours in our experiments)
- The computation time of a SBH schedule seems to be small enough to allow for application of this approach on a real shop floor

Multi-Objective Optimization using the Shifting Bottleneck Heuristic

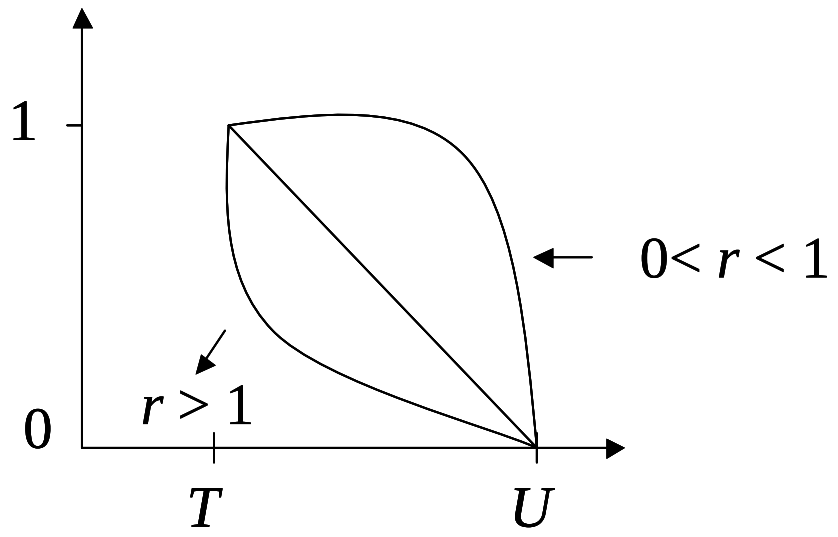
Dr. Michele Pfund, Hari Balasubramanian, Dr. John Fowler, Dr. Scott Mason, Dr. Oliver Rose

Pfund, M.E., Balasubramanian, H., Fowler, J.W., Mason, S.J. and Rose, O., 2008. A multi-criteria approach for scheduling semiconductor wafer fabrication facilities. *Journal of Scheduling*, *11*(1), pp.29-47.

Desirability Function Approach

- Derringer and Suich (1980)
- Main idea: to convert each objective into an individual desirability function d_i such that $0 <= d_i <= 1$
- Finally, combine all the desirabilities into a single function $D = (d_1 d_2 d_3 \ldots d_m)^{1/m}$
- It is possible to control the importance of each performance measure

The Desirability Function



$d = 1$, if $y < T$

$d = ((U - y)/(U - T))^{\wedge} r$,
if $T <= y <= U$

$d = 0$, if $y > U$

start delay

Desirability at the SSP Level

1. Vary ATCSR parameters (*k1, k2* and *k3*) to provide different schedules

2. Record the TWT, CT, Makespan values of all these schedules

3. For each measure calculate the upper (worst) and lower (best) values

4. Use the upper and lower values and the desirability weights to calculate the desirabilities of the schedules

5. Choose the schedule with the highest desirability

Desirability at the MCM-Level

- Local MCM approach: Choose the toolgroup with least desirability. This desirability is based on objective values at the SSP level.
- Global MCM approach: Insert each SSP schedule into the graph, calculate desirability of the overall schedule, and choose the least desirable toolgroup.
- In both these approaches, for each toolgroup store values of performance measures (Simple MCM: SSP values, Global MCM: Graph values)
- After iterating through all toolgroups, for each objective, set lower_bound = least value observed, and upper_bound = highest_value observed
- Using these bounds calculate desirabilities for each toolgroup, and choose the toolgroup with least desirability

Different Approaches

No.	SSP level	MCM level
1	Only TWT	Only TWT
2	Only TWT	Desirability (Local MCM)
3	Only TWT	Desirability (Global MCM)
4	Desirability	Only TWT
5	Desirability	Desirability (Local MCM)
6	Desirability	Desirability (Global MCM)

Testing

- Objectives: Makespan (translates to throughput), Cycle Time, and Total Weighted Tardiness
- Model used for testing: Modified Version of Testbed Dataset 1 on the MASM website.
- Number of jobs: 50
- Due-Dates: Set using flowfactor (FF) Due Date = release time + FF * raw process time
- In our testing FF~U(1,1.3) and weights U(1,100)

Results

	SSP-TWT	SSP-Des	SSP-TWT	SSP-TWT	SSP-Des	SSP-Des			
Instance	MCM-TWT	MCM-TWT	MCM-Des(G)	MCM-Des(L)	MCM-Des(G)	MCM-Des(L)	CR	EDD	FIFO
1	0.759	0.044	0.026	0.039	0.883	**0.982**	0.418	0.041	0.018
2	0.851	**0.968**	0.889	0.897	0.887	0.937	0.044	0.431	0.011
3	0.800	0.978	0.816	0.774	**0.995**	0.984	0.393	0.043	0.011
4	0.730	0.970	0.797	0.781	0.953	**0.995**	0.043	0.403	0.011
5	0.721	0.973	0.776	0.469	**0.999**	0.925	0.341	0.038	0.010
6	0.599	0.929	0.609	0.938	**0.973**	0.864	0.378	0.044	0.011
7	0.041	**0.989**	0.041	0.021	0.958	0.959	0.366	0.040	0.018
8	0.040	**1.000**	0.040	0.040	0.899	0.894	0.370	0.041	0.010
9	0.041	0.876	0.878	0.900	**1.000**	0.917	0.384	0.039	0.010
10	0.699	0.937	0.681	0.645	0.983	**0.984**	0.356	0.039	0.011
11	0.826	**0.990**	0.793	0.671	0.908	0.966	0.041	0.337	0.018
12	0.799	**0.970**	0.808	0.662	0.863	0.739	0.357	0.039	0.017
13	0.041	**0.997**	0.041	0.042	0.971	0.952	0.358	0.041	0.011
14	0.733	**0.933**	0.799	0.712	0.893	0.870	0.039	0.349	0.011
15	0.039	0.946	0.022	0.042	0.952	**0.973**	0.042	0.396	0.015
16	0.823	0.926	0.656	0.827	**0.978**	0.931	0.404	0.041	0.011
17	0.798	0.987	0.852	0.825	**0.998**	0.915	0.041	0.351	0.010
18	0.717	0.902	0.640	0.817	0.955	**0.963**	0.041	0.356	0.018
19	0.772	**1.000**	0.885	0.832	0.974	0.896	0.370	0.043	0.011
20	0.722	0.857	0.777	0.787	0.908	**1.000**	0.039	0.304	0.010
Ave	0.578	0.908	0.591	0.586	**0.947**	0.932	0.241	0.171	0.013
Std. Dev	0.323	0.208	0.339	0.342	**0.045**	0.061	0.168	0.165	0.003

Results

	TWT				CT				Makespan			
	SSP-TWT	Best of			SSP-TWT	Best of			SSP-TWT	Best of		
No.	MCM-TWT	Des App	CR	FIFO	MCM-TWT	Des App	CR	FIFO	MCM-TWT	Des App	CR	FIFO
1	60710.2	**38464.7**	77562.5	139552	414.2	**401.632**	421.783	447.406	516.067	**496.317**	515.1	536.833
2	67128.7	**44401**	74828.1	163917	411.703	**403.078**	418.885	447.406	510.867	**494.15**	513.617	536.833
3	89868.9	**57984.1**	89276.9	152002	424.269	**410.021**	419.607	447.406	518.283	**505.167**	522.467	536.833
4	51431.7	**35202.8**	65718.8	123925	419.551	**408.631**	428.067	447.406	523.067	**518.25**	525.95	536.833
5	95454.1	**70799.3**	91848.2	169196	419.104	**416.14**	420.548	447.406	528.483	**505.75**	522.017	536.833
6	75444.5	**66455.4**	84913.9	150170	411.031	**410.955**	415.514	447.406	524.15	**505.75**	510.017	536.833
7	71192.2	**53057.1**	83607	151919	413.887	**404.997**	420.368	447.406	520.35	**497.917**	516.917	536.833
8	85961.5	**70494.4**	100754	146034	417.221	**411.569**	421.043	447.406	536.417	**502.067**	520.75	536.833
9	59184.9	**44653.2**	68534.4	151999	412.779	**405.125**	418.721	447.406	526.9	**504.017**	515.333	536.833
10	66029.8	**39878.9**	75144.9	147151	414.735	**401.774**	419.654	447.406	523.517	**490.45**	519.417	536.833
11	62802.3	**49638.2**	65613.4	144419	410.728	**409.24**	411.8	447.406	523	**507.467**	501.017	536.833
12	57227.7	**54651.7**	75398.2	153022	412.564	**412.526**	421.319	447.406	524.05	**509.217**	512.9	536.833
13	70218.3	**61010.6**	83708.5	174919	408.08	**407.583**	416.852	447.406	529.083	**503.933**	509.9	536.833
14	82573.6	**70049.3**	88034	160210	417.457	**414.282**	419.689	447.406	525.55	**502.617**	515.3	536.833
15	61834.8	**34063.5**	68177.2	159809	415.807	**403.931**	422.535	447.406	521.667	**497.833**	515.733	536.833
16	72319.1	**54312.9**	73630.9	154704	415.443	**408.976**	418.416	447.406	531.9	**508.3**	521.3	536.833
17	69475.7	**36973.8**	59411.7	143170	419.315	**405.267**	417.792	447.406	522.133	**494.667**	514.05	536.833
18	71103.4	**43688**	68050.8	152419	414.029	**403.212**	414.315	447.406	521.633	**495.55**	511.65	536.833
19	80570.2	**62869.1**	79054.7	181314	412.687	**404.106**	416.438	447.406	521.05	**499.9**	517.65	536.833
20	87394.1	**64671.3**	93407	164421	418.741	**415.058**	421.809	447.406	529.25	**506.25**	524.2	536.833
Avg.	71896.285	**52665.965**	78333.755	154213.6	415.16655	**407.90515**	419.25775	447.406	523.87085	**502.27845**	516.26425	536.833

Some Selected Relevant Papers

- Mönch, L., Rose, O. and Sturm, R., 2003. A simulation framework for the performance assessment of shop-floor control systems. *Simulation*, 79(3), pp.163-170.
- Mason, S.J., Jin, S. and Wessels, C.M., 2004. Rescheduling strategies for minimizing total weighted tardiness in complex job shops. *International Journal of Production Research*, 42(3), pp.613-628.
- Mason, S.J., Fowler, J.W., Carlyle, W.M. and Montgomery, D.C., 2005. Heuristics for minimizing total weighted tardiness in complex job shops. *International Journal of Production Research*, 43(10), pp.1943-1963.
- Mönch, L. and Drießel, R., 2005. A distributed shifting bottleneck heuristic for complex job shops. *Computers & Industrial Engineering*, *49*(3), pp.363-380.
- Upasani, A.A., Uzsoy, R. and Sourirajan, K., 2006. A problem reduction approach for scheduling semiconductor wafer fabrication facilities. *IEEE Transactions on Semiconductor Manufacturing*, *19*(2), pp.216-225.

- Mönch, L. and Zimmermann, J., 2011. A computational study of a shifting bottleneck heuristic for multi-product complex job shops. *Production Planning and Control*, *22*(1), pp.25-40.
- Drießel, R. and Mönch, L., 2012. An integrated scheduling and material-handling approach for complex job shops: a computational study. *International Journal of Production Research*, *50*(20), pp.5966-5985.
- Yugma, C., Blue, J., Dauzère-Pérès, S. and Obeid, A., 2015. Integration of scheduling and advanced process control in semiconductor manufacturing: review and outlook. *Journal of Scheduling*, 18(2), pp.195-205.
- Waschneck, B., Altenmüller, T., Bauernhansl, T. and Kyek, A., 2016. Production Scheduling in Complex Job Shops from an Industry 4.0 Perspective: A Review and Challenges in the Semiconductor Industry. In *SAMI@ iKNOW* (pp. 1-12).
- Jamrus, T., Chien, C.F., Gen, M. and Sethanan, K., 2017. Hybrid particle swarm optimization combined with genetic operators for flexible job-shop scheduling under uncertain processing time for semiconductor manufacturing. IEEE Transactions on Semiconductor Manufacturing, 31(1), pp.32-41.
- Knopp, S., Dauzère-Pérès, S. and Yugma, C., 2017. A batch-oblivious approach for complex job-shop scheduling problems. *European Journal of Operational Research*, *263*(1), pp.50-61.

For more information

- Mönch, L., Fowler, J.W., Dauzere-Peres, S., Mason, S.J., Rose, O., “A Survey of Problems, Solution Techniques, and Future Challenges in Scheduling Semiconductor Manufacturing Operations”, *Journal of Scheduling*, Vol. 14, pp. 583-599, 2011.

- We are working on an update to this paper

Agenda

- Motivation
- Process Description
- Scheduling Problems
- Factory Scheduling **Part 1**

- Batch Scheduling Problems **Part 2**
- Multiple Orders per Job Scheduling Problems **March 16**
- Scheduling Jobs with Time Constraints
- Conclusions and Future Challenges